A new Logic Converter

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Abstract: special design for analog voltage-to-4 valued logic converter is implemented. In this study 2-bits converter was developed and tested using PLA (Programmable Logic Arrays) and two Digital-to-Analog converters.

Key words: Multiple valued logic, analog-to-digital converter

INTRODUCTION

One problem, which has not received considerable attention, in the past two-decades, in the area of multiple valued logic (MVL) , is the conversion of analog voltage into r-radix as quaternary. The engineering advantage of such design is essential to the new trend of MV logical family, which is proposing the design of decimal machine[1] and quaternary logic[2] .
Several papers have dealt with the development of quaternary circuits[2-4] for their advantage over binary circuits in their reduction of wiring and the increase in packing density of IC[5].

However, the area of development that will possibly leads to the general acceptance of MVL is the incorporation of MVL devices and circuits into mixed radix system, in conjunction with binary devices and circuits where their advantageous properties can be employed to the greatest effect. The future development of MVL circuits and systems, whether stand-alone or mixed radix, should be interesting and hopefully, profitable in many ways[6] .

In this study an analog-to-quaternary converter using CPLD was developed which is important to the development of several MV application in instrumentation and in signal processing techniques using MVL[7,8]. The design used a dual (binary)-to-four level (quaternary) converter. The conversion speed obtained for the simulated system was about 80ns.

Mathematical notation

Definition: The multiple valued logic algebra system is a system that has the following properties:

I. It has a set of m elements, denoted by M(m) where:
$$M(m) = \{0, 1, 2, \ldots, (m-l)\}$$
With $0 < l < 2 \ldots < (m-l)$.

II. Quaternary variable has four logical values $\{0, 1, 2, 3\}$. In this study, the logical values 0,1,2and 3 are expressed by specific voltages shown in Table 1.

Design approach: A block diagram to represent the main elements for the A/Q converter is shown in Fig. 1, the first stage is comprised of the analog comparators which are used to generate binary output (0,1) based on the comparison of Vi and the reference voltage V_{ref}. Reference voltage equations are derived using voltage divider rule based on the radix input and the number of bits as shown below:

$$V_1 - (4^n - 1)V_{ref}/4^n$$
$$V_2 = (4^n - 2) V_{ref}/4^n$$
$$V_n = V_{ref}/4^n$$

The number of Comparators (Q) required are calculated using the following relationship:

$$Q = 4^n - 1 \qquad (1)$$

where n: number of converter output digits.

Table 1: Logical Values and their corresponding voltages

Logical value	0	1	2	3
Voltage (V)	-4.5	-1.5	1.5	4.5

For example: quaternary of2-digit converter requires 15-comparators.

The generated data from the comparators are fed to the encoder circuit, which can generate binary output (Y) of :
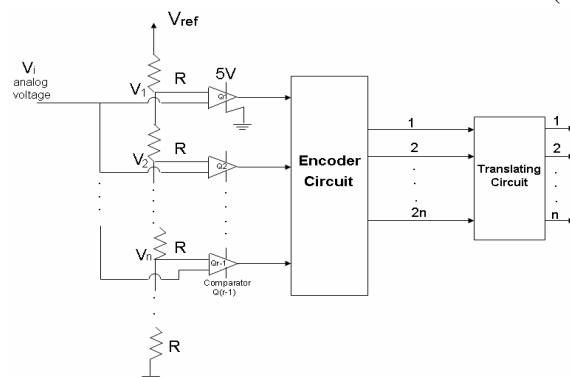
$$Y = 2n \qquad (2)$$

Fig. 1: Block diagram to A/Q converter

In the example introduced, the 2-digits converter, the number of encoder outputs is 2x2=4. Table 3 shows the input and the output of the encoder listing the output as $(Y_i, Y_2, Y_3$ and $Y_4,)$. The design of this encoder is based on the standard design technique for implementing binary digital system of encoders[9].

Other and easier, method for encoder implementation is the use of programmable logic array (PLA) as shown in Fig. 2 this implementation requires CPLD programming.
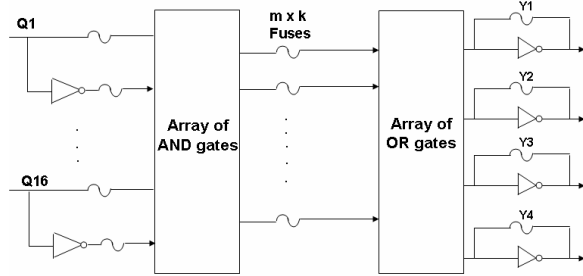

Fig. 2: PLA implementation of the encoder circuit using CPLD

The third section is a translating circuit consists of Dual input (binary)-to-four level converter (quaternary). Figure 3 shows the designed circuit. The four resistors value associated with Ul and U2 are used to set the compare level to +2.5 volt DC (1/2 Vcc). When the input bit level is less than +2.5 volts DC (binary 0), the Comparator will output one level (+5V) and when the input bit level is greater than +2.5 Volt DC (binary 1), the Comparator will output the other level (-5 V). The output from Ul and U2 are then proportionally summed together by U3. The output voltage X of U3 is found from the adder equation:

$$X = - R_f [E1/R1 + E2/2R1] \qquad (3)$$

In a simplified example, where Yl=l and Y2=0, the input binary to Ul is greater than the compared level indicating a high level. But the Yl bit is applied to the inverting input so that El becomes a -5 volts DC. The Y2 bit is input to the non-inverting terminal, so that when Y2 =0, the E2 output voltage will be -5 Volt DC also. From equation 3, X= -R_f[5/rl-5/2rl] which is equal to +1.5volt DC for R1=5K and R_f=3k. The other 3-combination using the same reasoning the output levels generated will be listed in Table 2.
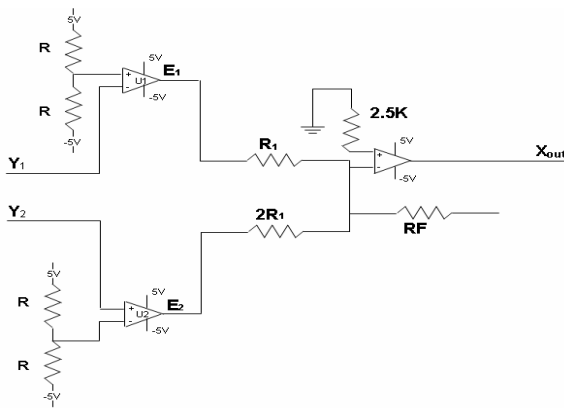

Fig. 3: Dual input (binary)-to four level (quaternary) converter

Table 2: Dual input (binary)-to four level (quaternary) converter for the circuit of Fig. 3

X (volts DC)	E2	E1	Y2	Yl
-4.5	-5	-5	0	1
-1.5	+5	-5	1	1
+1.5	-5	+5	0	0
+4.5	+5	+5	1	0

Flash A/Q converter: The flash analog to quaternary converter implemented to demonstrate the model introduced .Table 3 shows a complete truth table for the 2-digits A/Q converter. V_{in} represent the analog voltage level and the output is made from two digits each of a different weight (0,1,2, 3).For 2-digits A/Q the number of comparators are calculated using equation (I): 4^2 - 1=15. The comparators output (Q1,Q2,..., Q_{16}) are either zero or one logic based on the V_{in} and the V_{ref} values .These outputs are listed in Table 3. The generated comparator outputs are fed to an encoder circuit .

The number of encoder outputs (Y_1, Y_2, Y_3 and Y_4) are calculated based on equation (2): 2x2=4 .The outputs are also zero or one logic generated for the corresponding inputs resulted from the comparison.

Figure 2 shows a complete circuit design for the digital (binary) encoder used for this A/Q converter, which is implemented using CPLD logic circuit.

The encoder output is finally translated to their corresponding multiple logical values as been defined in Table 2. In this case a two-digit quaternary output converter will require two Binary-to -Quatemary converter circuits similar to the circuit shown in Fig. 3. The output of the two (XI ,X2) binary-to-quatemary circuits will generate 16 different MV logical combinations as listed in Table 3.

CONCLUSION

The circuit was simulated and tested with successful result. The response time for the circuit is determined by the Comparator input to output transfer delay plus the worst case propagation delay through binary encoder and the output translating circuit. The Comparator response time =10 ns .The binary encoder is comprised a PLA device which was implemented in VHDL (Very High Speed Application Specific Integrated Circuit Hardware Description Language) using MAX+PLUS II software. This and the translating binary-to-quatemary OP-Amps will give together a propagation delay of around 70ns. However the speed of conversion can be improved by employing faster digital encoder and higher speed components as ECL binary logic. A drawback to the system is its complexity for higher radix and greater output digits, especially when higher outputs digits is needed, for example: an 8-digits A/Q converter requires 4^8-1 comparators, more complicated digital encoder and eight D/A circuits. However this approach can be

Table 3: Truth table for Analog-to-quaternary converter

V_{in}	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Y1	Y2	Y3	Y4	X1	X2
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0.4	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0.8	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2
1.2	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	3
1.6	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
2.4	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	2
2.8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	3
3.2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	2	0
3.6	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	1	2	1
4	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0	2	2
4.4	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1	2	3
4.8	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0	3	0
5.2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	1	3	1
5.6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	3	2
6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3	3

studied further for higher radix converter as the special-purpose MV logic computer (decimal machine) or include a study for computer modeling to the system (further work is developed by the author).

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